5560028

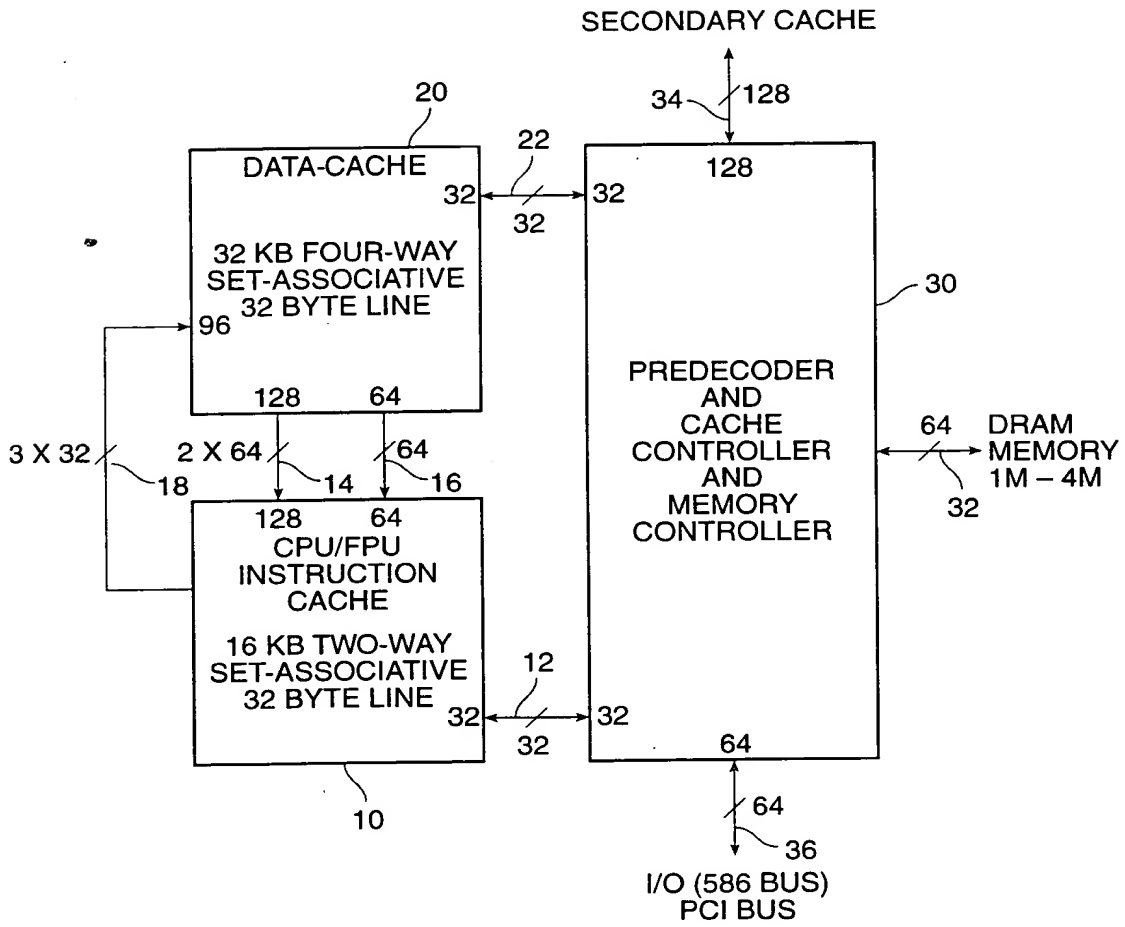

FIG. 1

FIG. 2

FIG. 3

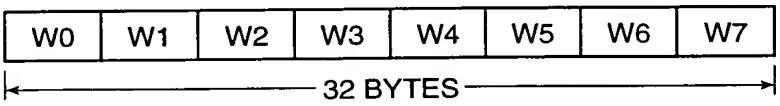

FIG. 4

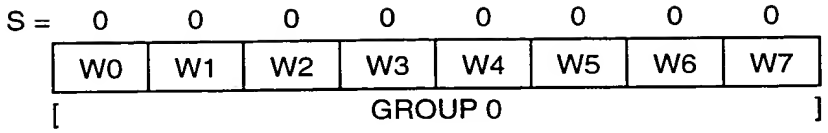

FIG. 5A

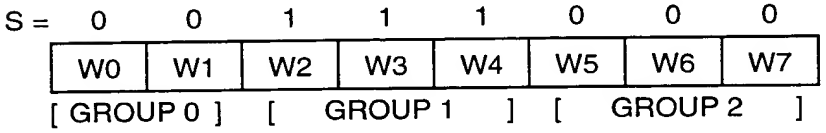

FIG. 5B

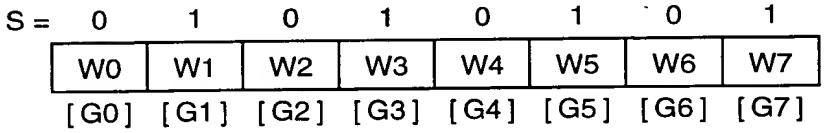

FIG. 5C

FIG. 6

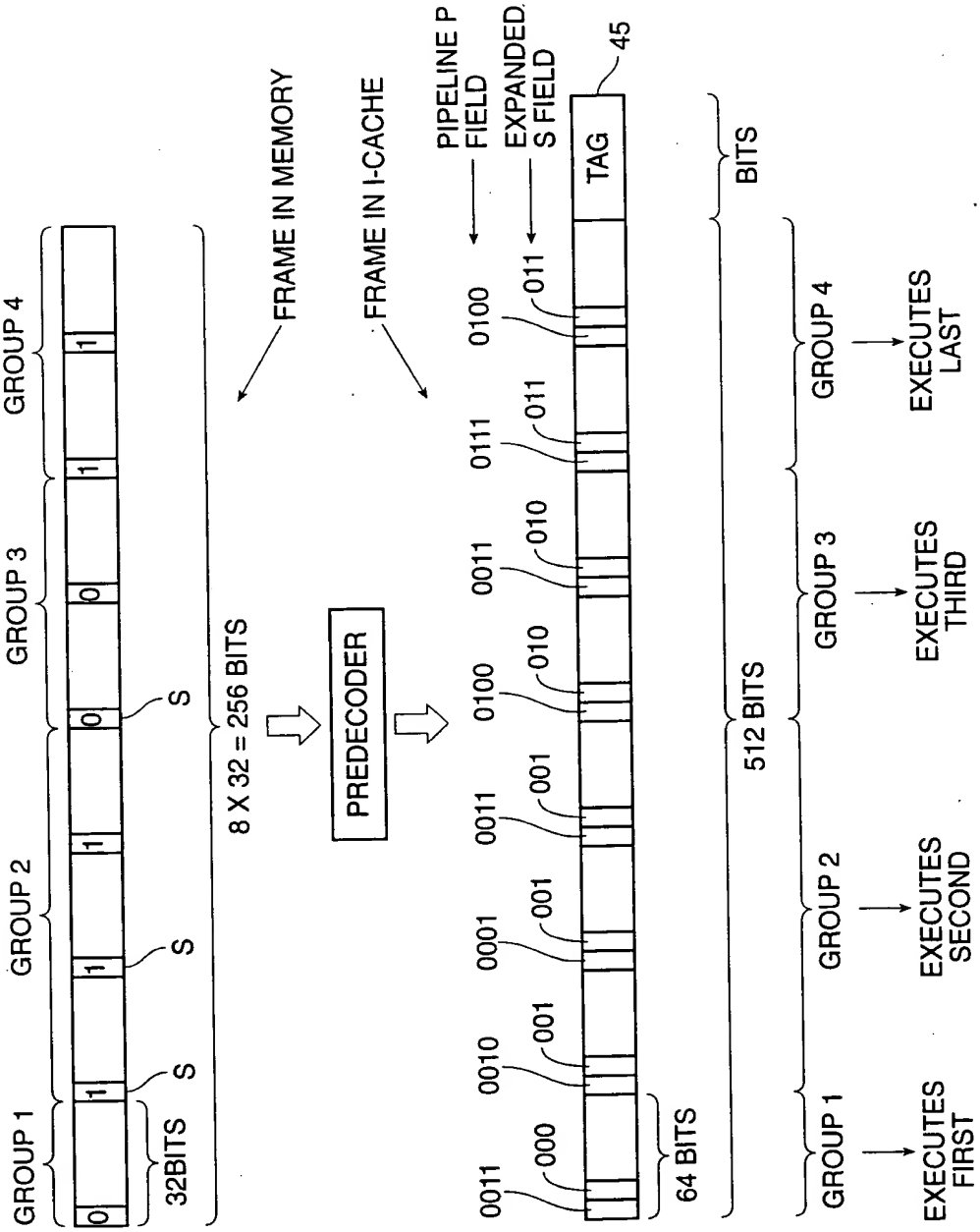
GROUP 1
GROUP 2
GROUP 3
GROUP 4
32BITS
S
S
S
8 X 32 = 256 BITS
FRAME IN MEMORY
PREDECODER
FRAME IN I-CACHE
PIPELINE P FIELD
EXPANDED S FIELD
TAG
45
0011
0010
0001
0100
0011
0111
0100
000
001
001
010
001
010
011
011
64 BITS
512 BITS
BITS
GROUP 1
GROUP 2
GROUP 3
GROUP 4
EXECUTES FIRST
EXECUTES SECOND
EXECUTES THIRD
EXECUTES LAST

FIG. 7

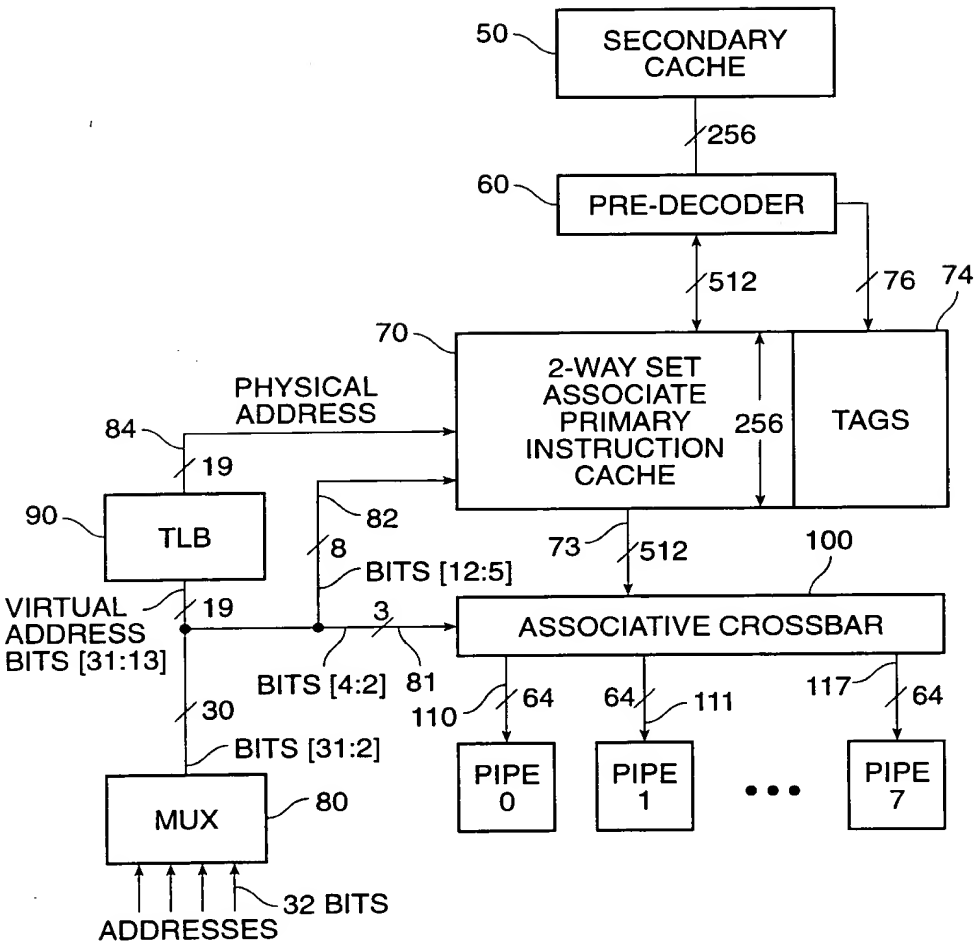
50
SECONDARY CACHE
256
60
PRE-DECODER
512
76
74
70
2-WAY SET ASSOCIATE PRIMARY INSTRUCTION CACHE
256
TAGS
PHYSICAL ADDRESS
84
19
90
TLB
82
8
BITS [12:5]
73
512
100
VIRTUAL ADDRESS BITS [31:13]
19
3
ASSOCIATIVE CROSSBAR
BITS [4:2]
81
110
64
64
111
117
64
30
BITS [31:2]
PIPE 0
PIPE 1
PIPE 7
MUX
80
32 BITS
ADDRESSES

FIG. 8

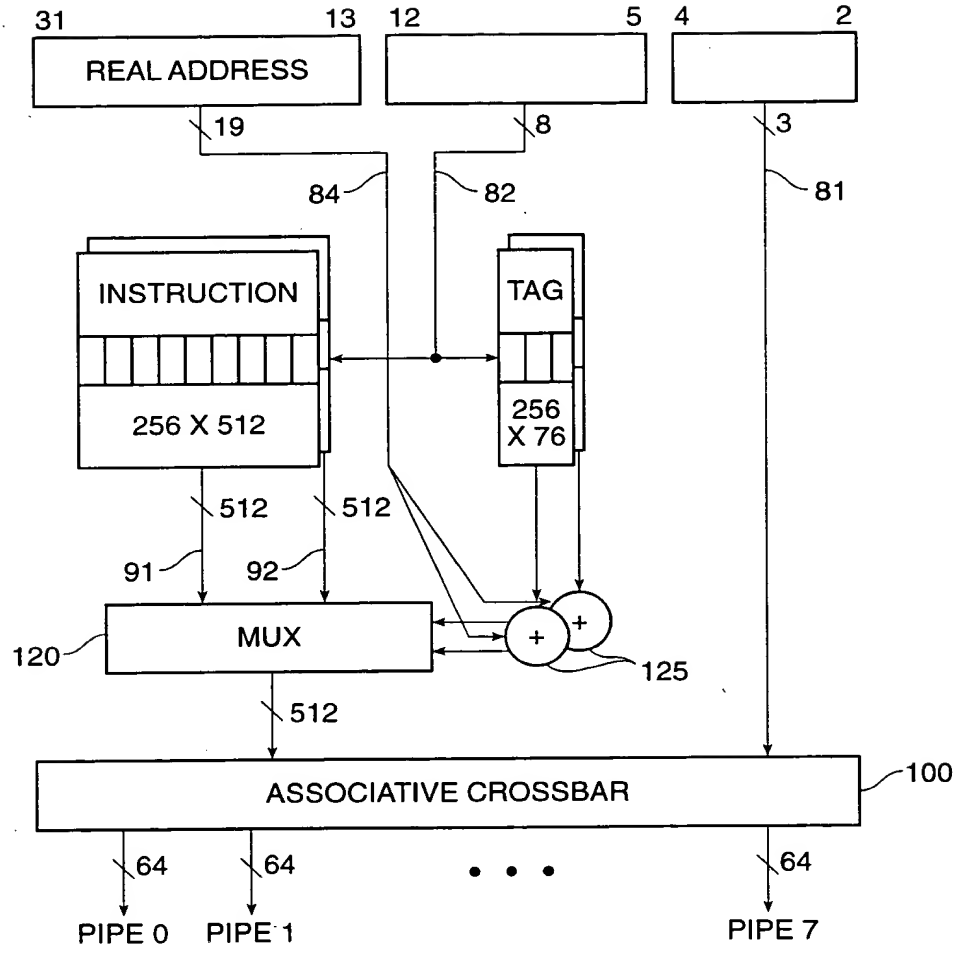
31
13
12
5
4
2
REAL ADDRESS
19
8
3
84
82
81
INSTRUCTION
256 X 512
TAG
256
X 76
512
512
91
92
MUX
120
+
+
125
512
ASSOCIATIVE CROSSBAR
100
64
64
64
PIPE 0
PIPE 1
PIPE 7

FIG. 9

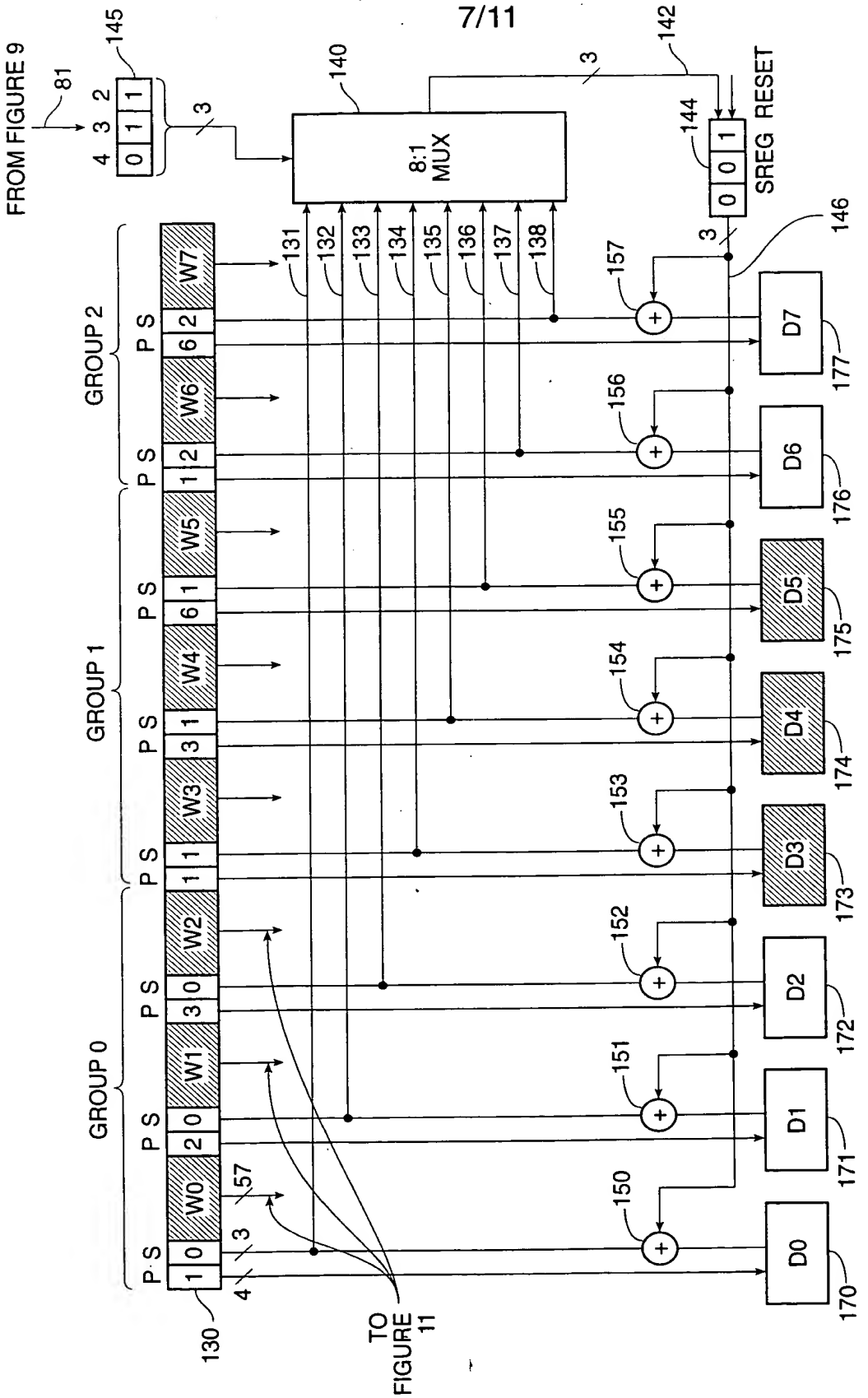
FROM FIGURE 9
81
145
4 3 2
0 1 1
3
140
8:1 MUX
3
142
144
0 0 1
SREG RESET
146
GROUP 0
GROUP 1
GROUP 2
P S
W0
W1
W2
W3
W4
W5
W6
W7
130
131
132
133
134
135
136
137
138
57
3
4
TO FIGURE 11
150
151
152
153
154
155
156
157
D0
D1
D2
D3
D4
D5
D6
D7
170
171
172
173
174
175
176
177

FIG. 10

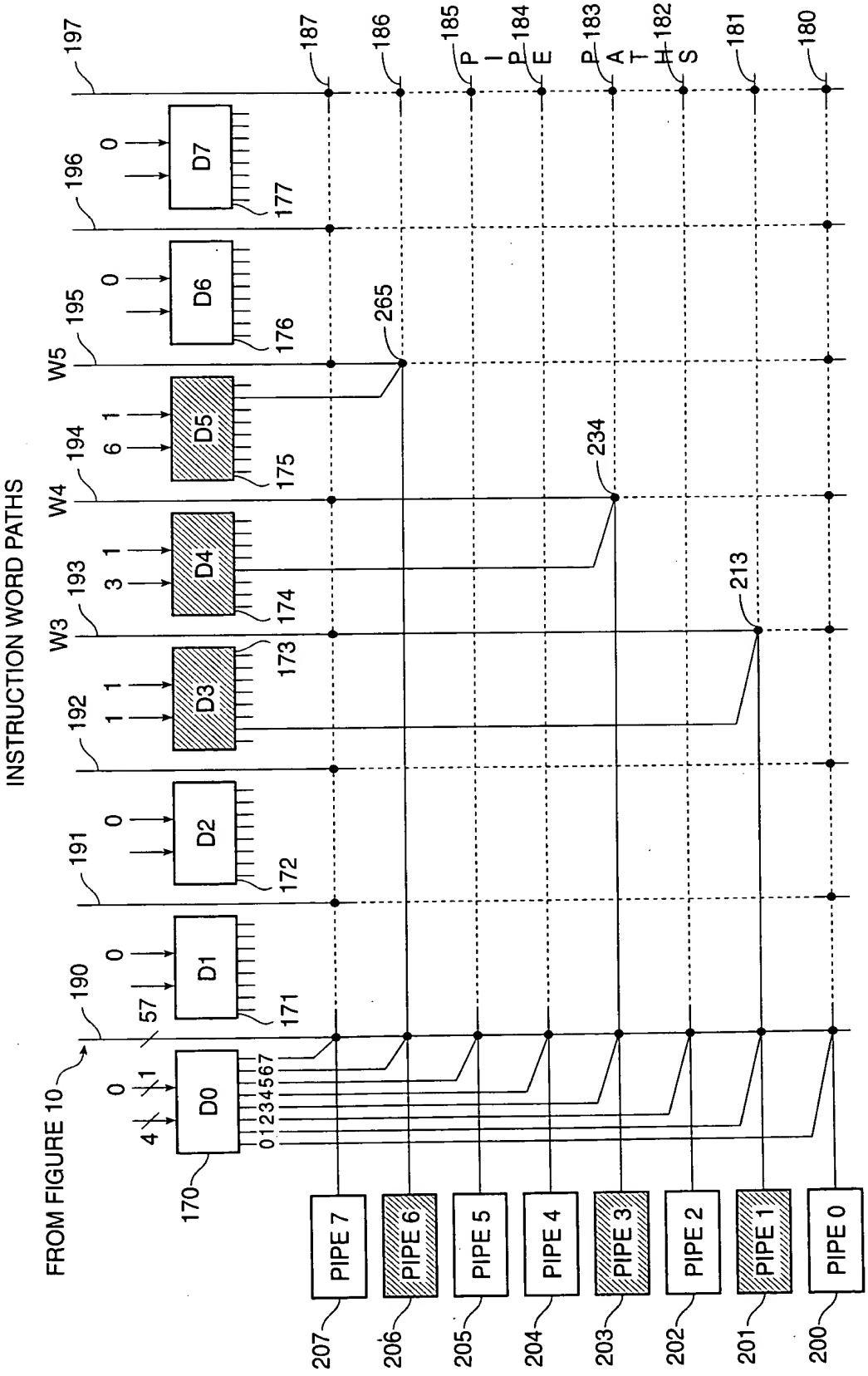
INSTRUCTION WORD PATHS
FROM FIGURE 10
D0
D1
D2
D3
D4
D5
D6
D7
PIPE 7
PIPE 6
PIPE 5
PIPE 4
PIPE 3
PIPE 2
PIPE 1
PIPE 0
PIPE STAGES
W3
W4
W5
265
234
213

FIG. 11

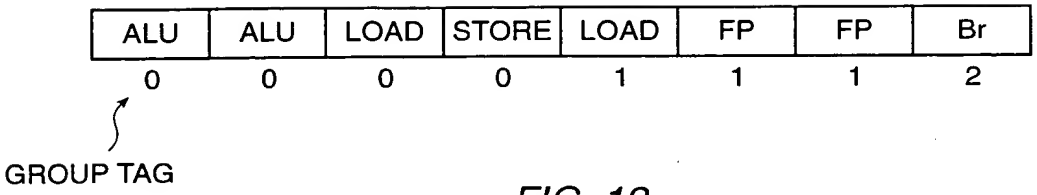

FIG. 12

CLOCK 1 —	ALU	ALU	LOAD	STORE
CLOCK 2 —	LOAD	FP	FP	
CLOCK 3 —	BRANCH			

FIG. 13

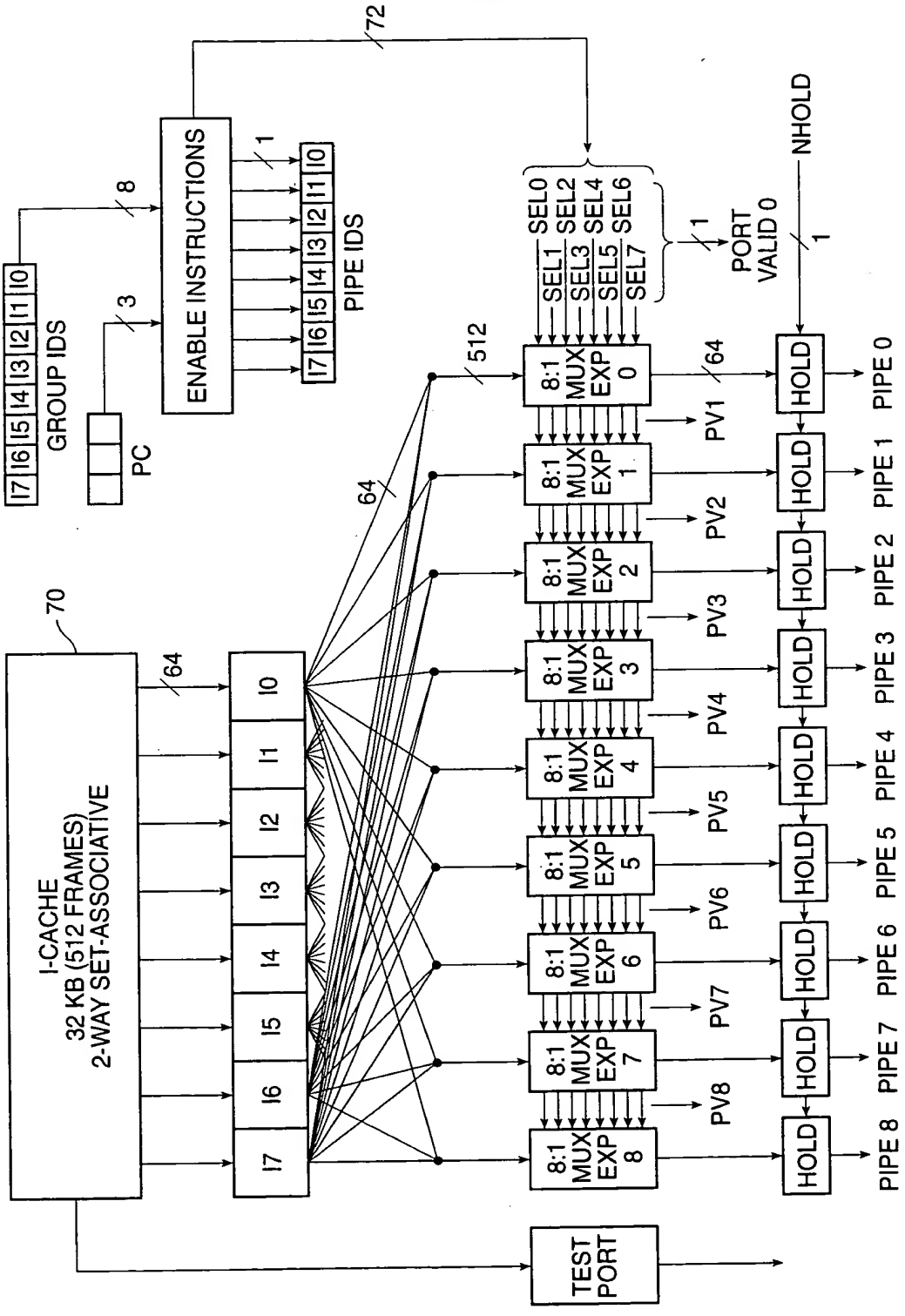
I-CACHE
32 KB (512 FRAMES)
2-WAY SET-ASSOCIATIVE
70
64
I0
I1
I2
I3
I4
I5
I6
I7
TEST PORT
GROUP IDS
I7 I6 I5 I4 I3 I2 I1 I0
8
PC
3
ENABLE INSTRUCTIONS
72
1
PIPE IDS
I7 I6 I5 I4 I3 I2 I1 I0
64
512
SEL0 SEL1 SEL2 SEL3 SEL4 SEL5 SEL6 SEL7
1
PORT VALID 0
NHOLD
1
8:1 MUX EXP 0
8:1 MUX EXP 1
8:1 MUX EXP 2
8:1 MUX EXP 3
8:1 MUX EXP 4
8:1 MUX EXP 5
8:1 MUX EXP 6
8:1 MUX EXP 7
8:1 MUX EXP 8
PV1
PV2
PV3
PV4
PV5
PV6
PV7
PV8
64
HOLD
PIPE 0
PIPE 1
PIPE 2
PIPE 3
PIPE 4
PIPE 5
PIPE 6
PIPE 7
PIPE 8

FIG. 14

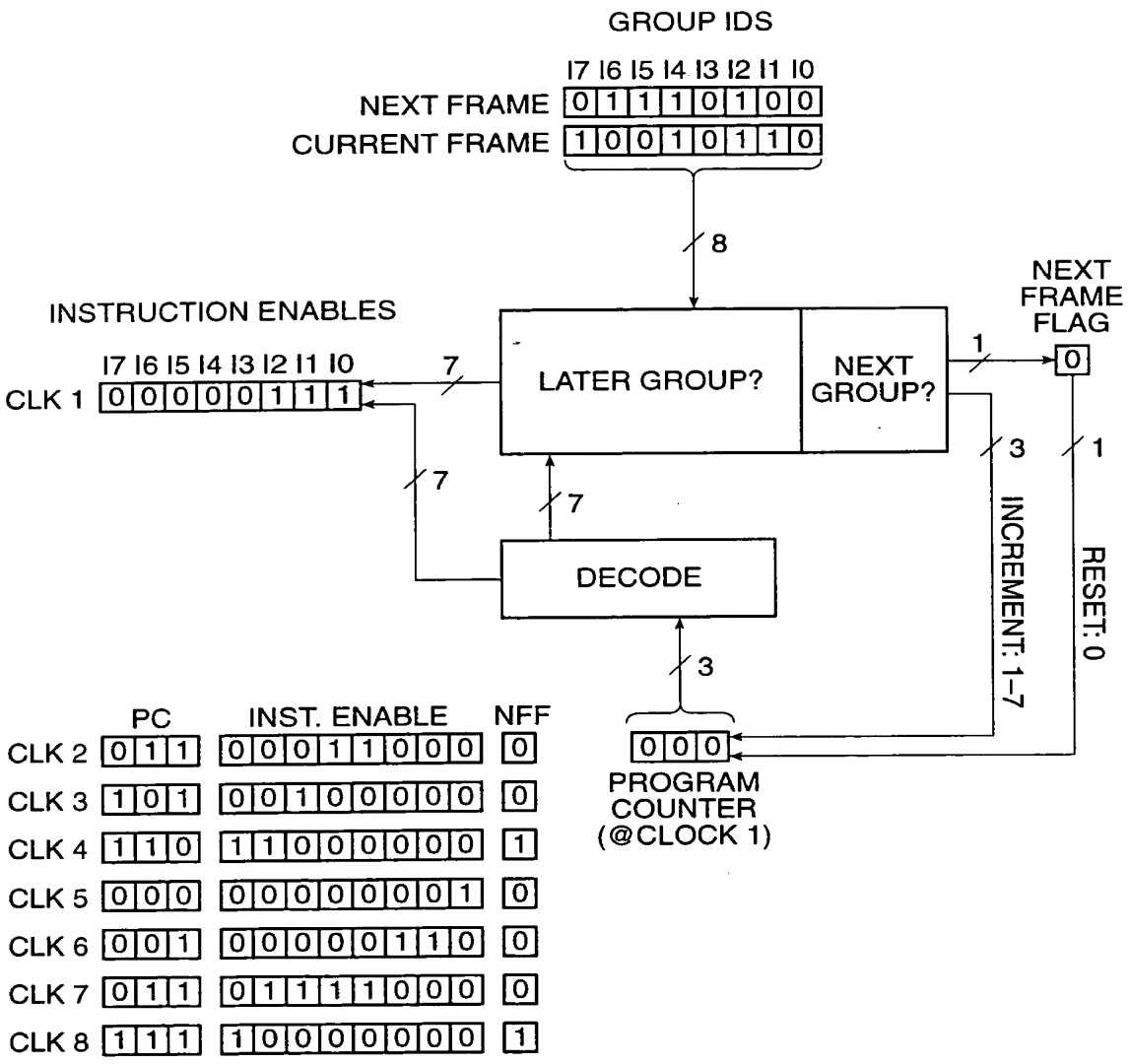
GROUP IDS
I7 I6 I5 I4 I3 I2 I1 I0
NEXT FRAME 0 1 1 1 0 1 0 0
CURRENT FRAME 1 0 0 1 0 1 1 0
8
INSTRUCTION ENABLES
I7 I6 I5 I4 I3 I2 I1 I0
CLK 1 0 0 0 0 0 1 1 1
7
LATER GROUP?
NEXT GROUP?
1
NEXT FRAME FLAG
0
3
1
7
7
INCREMENT: 1–7
RESET: 0
DECODE
3
0 0 0
PROGRAM COUNTER (@CLOCK 1)
PC
INST. ENABLE
NFF
CLK 2 0 1 1 0 0 0 1 1 0 0 0 0
CLK 3 1 0 1 0 0 1 0 0 0 0 0 0
CLK 4 1 1 0 1 1 0 0 0 0 0 0 1
CLK 5 0 0 0 0 0 0 0 0 0 1 0
CLK 6 0 0 1 0 0 0 0 0 1 1 0 0
CLK 7 0 1 1 0 1 1 1 1 0 0 0 0
CLK 8 1 1 1 1 0 0 0 0 0 0 0 1

FIG. 15